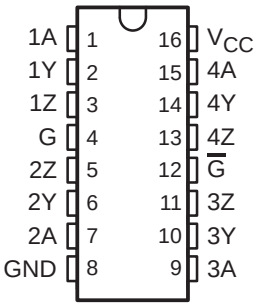
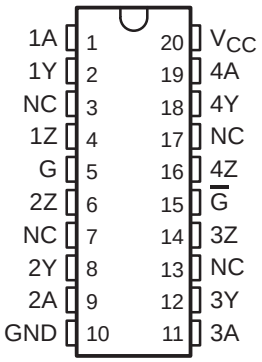
- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Active-High and Active-Low Enables**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Operates From Single 5-V Supply**
- **Logically Interchangeable With AM26LS31**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75172 is a monolithic quadruple differential line driver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. The device is optimized for balanced multipoint bus transmission at rates of up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges, making it suitable for party-line applications in noisy environments.

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75172 is characterized for operation from 0°C to 70°C.

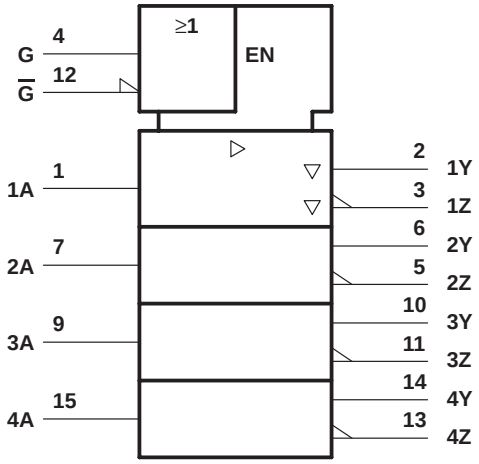
FUNCTION TABLE
(each driver)

INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

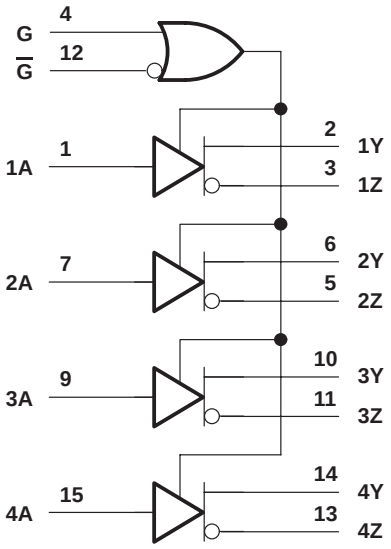
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Terminal numbers shown are for the N package.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage range at any bus terminal . . . . . –10 V to 15 V
Input voltage, V_I . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			–7 to 12	V
High-level output current, I_{OH}			–60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA					–1.5	V
V_O	Output voltage	I_O = 0			0		6	V
V_{OH}	High-level output voltage	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OH} = –33 mA		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OH} = 33 mA		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0			1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1		1/2 V_{OD1} or 2‡			V
		R_L = 54 Ω,	See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 2			1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,		See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage¶						+3 –1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§						±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = – 7 V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = – 7 V to 12 V					±100	µA
I_{IH}	High-level input current	V_I = 2.7 V					20	µA
I_{IL}	Low-level input current	V_I = 0.5 V					–360	µA
I_{OS}	Short-circuit output current	V_O = – 7 V					–180	mA
		V_O = V_{CC}					180	
		V_O = 12 V					500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			38	60	mA
			Outputs disabled			18	40	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 2: See Figure 3-5 of EIA Standard RS-485.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD2}\|$		V_t (Test Termination) Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|,\|I_{sb}\|$	
I_O	$\|I_{xa}\|,\|I_{xb}\|$	I_{ia},I_{ib}

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω,	See Figure 2		45	65	ns
$t_{t(OD)}$	Differential-output transition time				80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 4		45	80	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 3		78	115	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 4		18	30	ns

PARAMETER MEASUREMENT INFORMATION

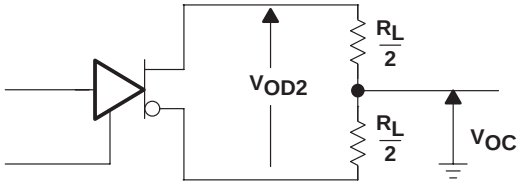
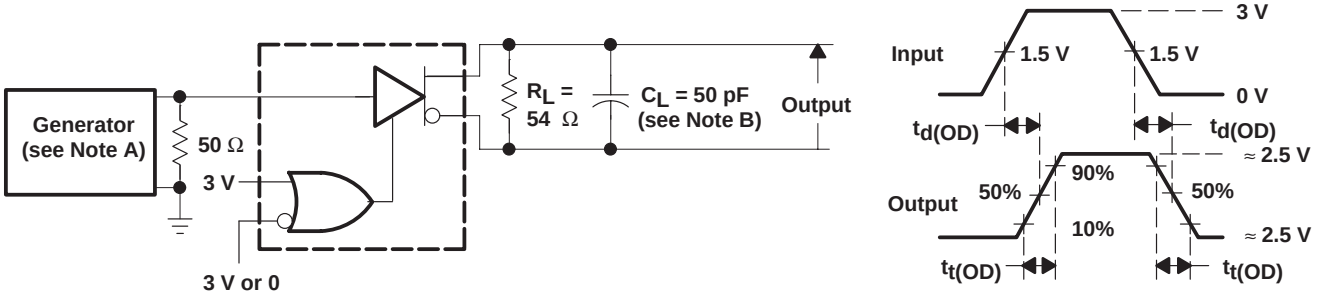


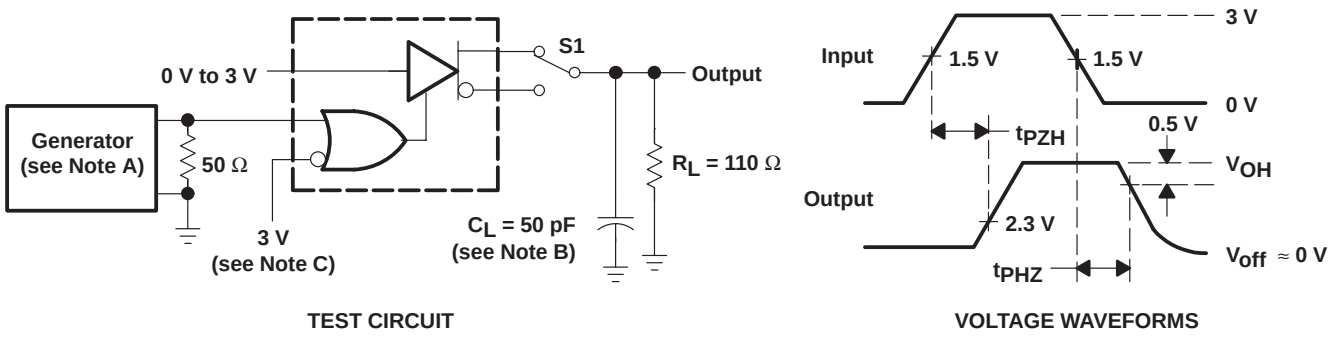
Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

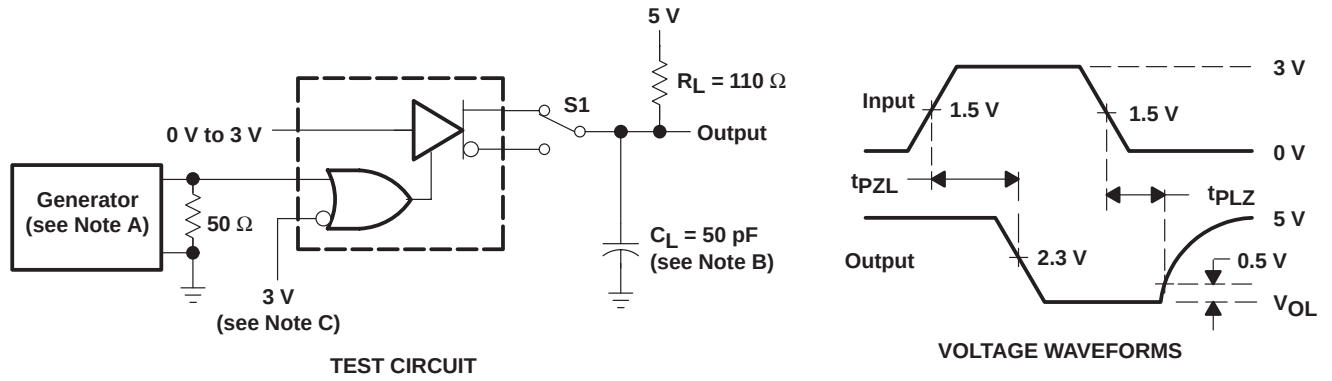
Figure 2. Differential-Output Test CIrcuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES. A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 3. Test Circuit and Voltage Waveforms



NOTES. A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

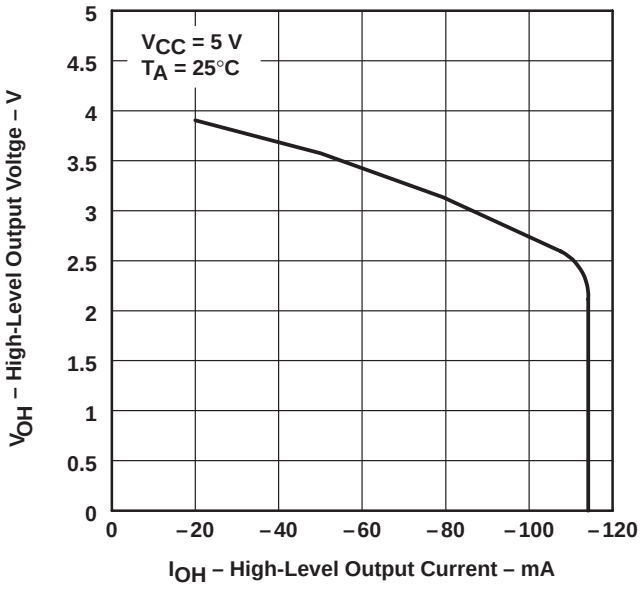


Figure 5

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

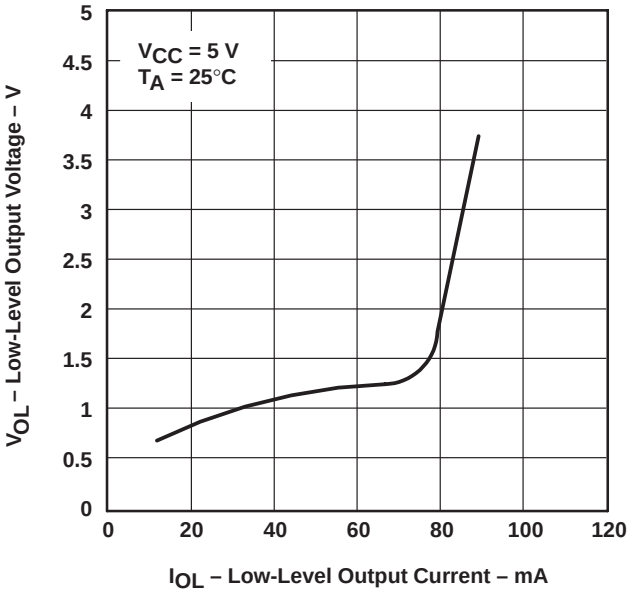


Figure 6

DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT

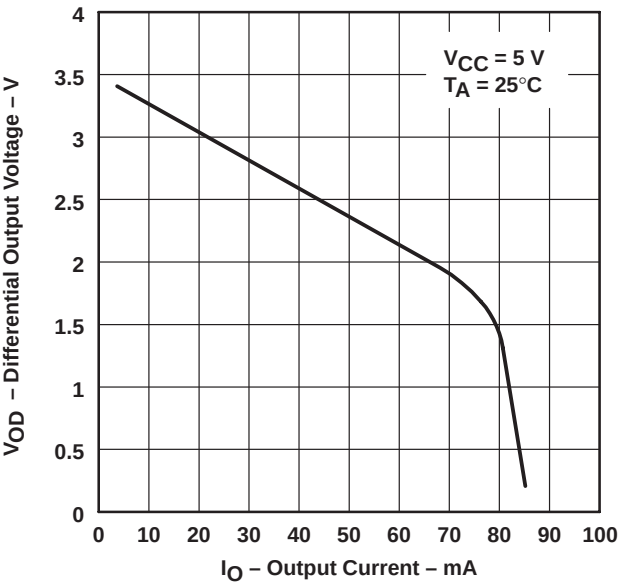


Figure 7

OUTPUT CURRENT vs OUTPUT VOLTAGE

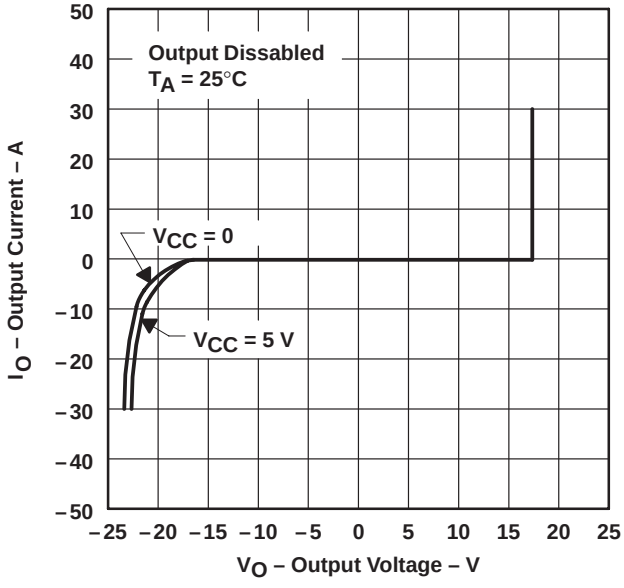


Figure 8

TYPICAL CHARACTERISTICS

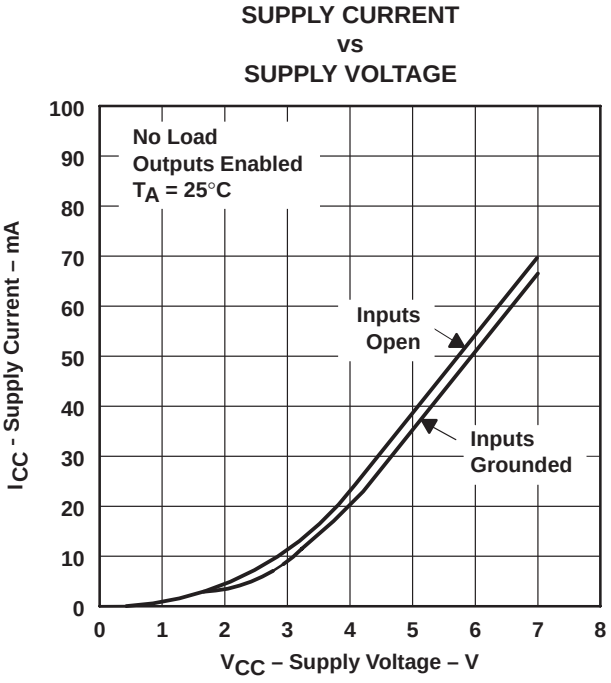


Figure 9

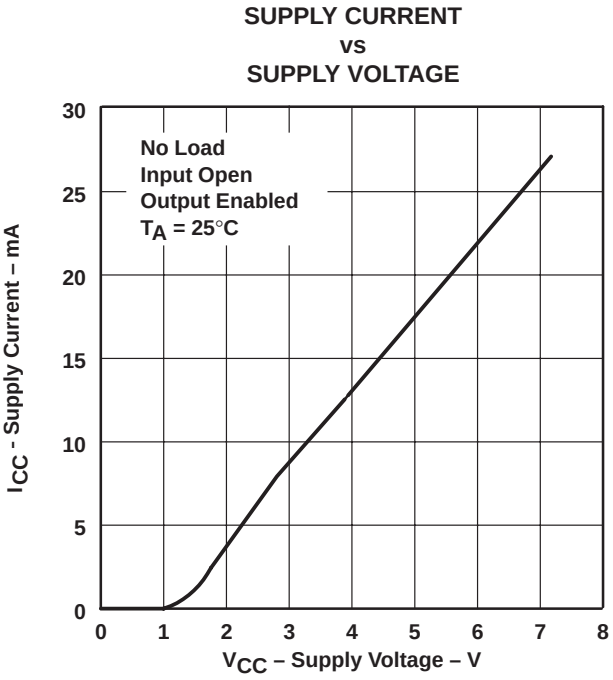
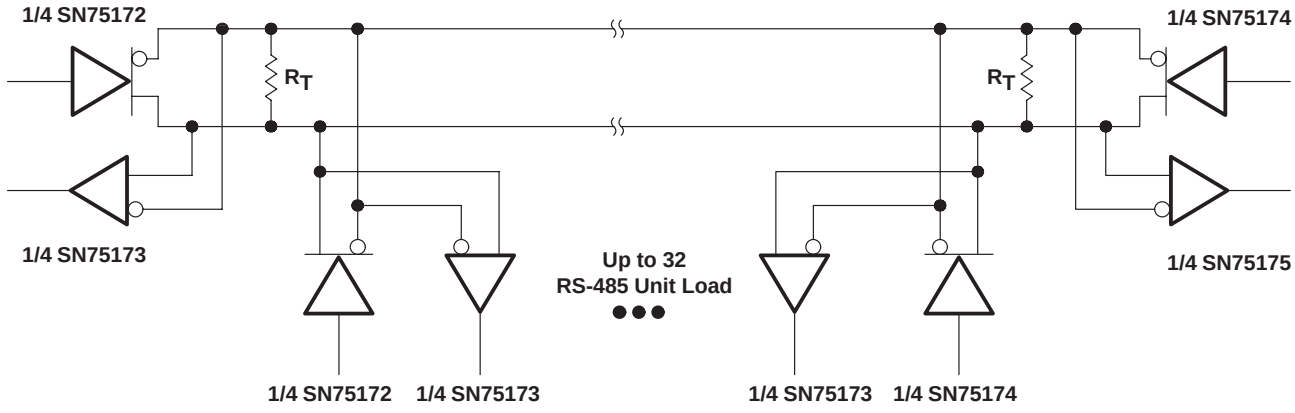


Figure 10

APPLICATION INFORMATION



NOTE A: The line length should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 11

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current and complete.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.